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(54) Wholly-digital demodulation system for QAM signalling in low capacity links.

(57) The present invention relates to a QAM signal demodulation system able to: recovery phase and frequency of the carrier and baseband convert the signal, also when frequency errors are remarkable with respect to the frequency of symbol (low capacity links); reconstruct the synchronism of symbol for correctly sampling the analog signal to be processed; complete the shaping of the signal through a digital filter and equalize the baseband converted signal (in order to undo the selective fading effects due to propagation and the linear distortions due to imperfections in the realization of the apparatus).

Therefore the system comprises several subsystems devoted to the performing of the various functions and, in particular, at least:

A) a carrier frequency and phase recovery subsystem,

B) a subsystem for reconstructing the synchronism of the symbol capable of driving the signal sampling circuit,

C) a subsystem constituted of filters.

The present invention is concerned with the choice of the particular subsystem used, their implementation and their interconnections.

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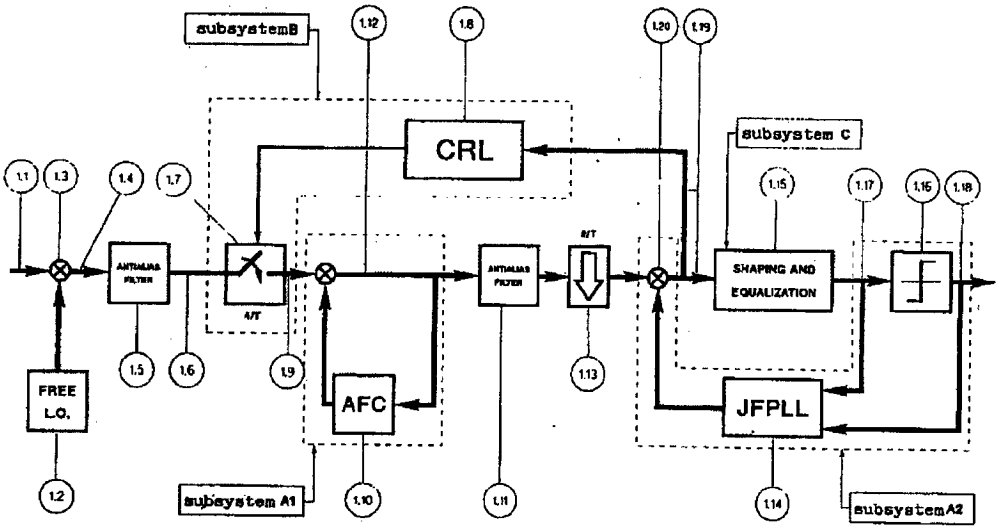
subsystemB
1.12
1.8
1.20
1.19
CRL
subsystem C
1.1
1.3
1.4
1.7
1.15
1.17
1.16
1.18
ANTIALIAS FILTER
A/T
ANTIALIAS FILTER
A/T
SHAPING AND EQUALIZATION
1.5
1.6
1.9
1.13
FREE LO.
AFC
JFPLL
1.2
subsystem A1
1.10
1.11
1.14
subsystemA2

Fig. 1

The present invention relates to a system for demodulating QAM signals, able to:

- recovery carrier phase and frequency and convert the baseband signal, also when the frequency errors are remarkable with respect to the frequency of symbol (low capacity links);
- reconstruct the synchronism of the symbol in order to correctly sample the analog signal to be processed;
- complete the shape of the signal through a digital filter and equalize the baseband converted signal (in order to undo the selective fading effects due to propagation and the linear distortions due to imperfections in realizing the apparatus).

Therefore the system is composed of several subsystems devoted to the carrying out of the various functions, and in particular of at least:

A) a subsystem for recovering phase and frequency of the carrier,

B) a subsystem for reconstructing the synchronism of the symbol capable of driving the signal sampling circuit,

C) a subsystem composed of filters.

The present invention concerns the choice of particular subsystems used, their implementation and interconnections. The system in accordance with the invention features the following characteristics.

a) Said system for recovering the carrier in turn comprises two subsystems: a four-correlator subsystem A1 for recovering the carrier frequency and a subsystem A2 for jointly recovering phase and frequency of the carrier that uses the estimated data. The two subsystems are cascade connected and each is structured as a feedback loop.

b) Subsystem B) uses the signal at the input of the subsystem C) and includes the circuit (placed upstream of subsystem A1) used for sampling the signal entering the system and converting it into a digital one. Subsystem B) is based on a maximum power algorithm; this implies that its operation is independent of the behaviour of the subsystem A) (because the algorithm is insensitive to the phase of the processed signal and therefore to errors in constructing phase and frequency of the carrier) and also from the one of subsystem C) (because the algorithm does not use the definite symbols).

c) Subsystem C) comprises a fixed digital filter which completes the shaping of the transmitted pulse and an adaptive digital equalizer. For both, the structure of Finite Impulse Response (FIR) filters has been chosen because they are particularly easy to implement. The equalizer coefficients are updated through an algorithm insensitive to the phase of the incoming signal so that its convergence is independent of the carrier recovery carried out by subsystem A).

The system according to the invention has now at least three basic advantages:

- it is not necessary to use a voltage controlled oscillator (VCO) to carry out the baseband conversion, but a free oscillator is sufficient;
- both the subsystems and their interconnections maintain their validity and effectiveness in a wide range of low/medium capacity links;
- single components and the demodulator as a whole are suitable for a wholly digital implementation that allows to minimize interconnection problems of analog and digital functional blocks; moreover the digital realization along with adaptivity of the subsystems make the calibration of the apparatus much less critical during the production.

STATE OF THE ART

Typically in coherent-demodulation systems, e.g. with quadrature amplitude modulation (QAM), local voltage controlled oscillators (VCOs) are used and driven in such a way as to generate an oscillation in phase and frequency coherence with the carrier of the received signal. The possibility of using free local oscillators having a frequency close to the carrier one would mean a remarkable advantage in terms of cost. However, such oscillators have tolerances different from zero on the nominal frequency and drift both with heat and aging. This requires a device which recognizes the frequence and phase difference between the oscillation generated by the local oscillator and the carrier of the signal and is capable of correcting the effects on the signal to be processed. The devices of this kind (phase and frequency locked loops) are characterized, inter alia, by the lock-in band, i.e. by the amount of frequency errors which they are able to recognize and correct. They belong to two main categories:

- devices that make use of estimates of the received data (having lock-in band smaller than one eigth of the frequency of symbol);
- devices that do not make use of estimates of the received data (having lock-in bands even greater than the frequency of symbol but are sensitive to selective fading).

The problem of tolerance and instability of the free oscillators is difficult to solve for small capacity links for which the frequency of symbol is lower and therefore the ratio of the frequency error to the frequency of symbol itself is higher.

If, on the other hand, links having capacity increasing gradually are considered, the spectral

occupation or the number of modulation levels and hence the sensitivity of the system to selective fading are increased. Consequently the introduction of an adaptive equalizer for counterbalancing the effects becomes necessary. This device constitutes a countermeasure against fading, but at the same time it is able to correct the linear distortions inevitably introduced in the realization of the system because of non-idealness of components. Therefore the introduction of the equalizer makes the system stronger with respect to anomalies in propagation, but it implies also a less critical calibration step: for this reason an equalizer (even if with few coefficients) is desirable also in the design of a low capacity system.

Moreover, in any demodulation system, it is necessary to insert a device for recovering the clock synchronism in phase and frequency. For the correct operation of the system, it is convenient that the algorithm for the clock recovery is independent of the behaviour of devices for carrier recovery and adaptive equalization.

In a digital modem, the clock synchronism is used to drive the signal sampling circuit with a suitable frequency, multiple of the frequency of symbol.

It is an object of the present invention to provide a solution for the above-mentioned problems having, inter alia, the advantages mentioned at the outset.

GENERAL SOLUTION

* Description of the system

The overall structure of the demodulator is described in the functional block diagram of fig. 1.

The radiofrequency analog signal (1.1) is baseband converted through multiplication with a sinusoidal oscillation generated by the free local oscillator (1.2) whose tuning frequency is nominally equal to the carrier frequency.

The outgoing complex signal (1.4) from the mixer (1.3) is filtered by anti-aliasing filter (1.5) in such a way as to limit the noise power at the subsequent stages.

Subsequently the analog signal (1.6) is converted into a numeric signal by sampler (1.7) which, on command of the outgoing signal from clock recovery loop (CRL) 1.8, samples the analog signal (1.6) at frequency 4/T, where 1/T is the signalling symbol frequency (subsystem B). This choice of the sampling frequency is connected to the frequency errors (introduced on signalling by non-idealness of the free oscillator) which can be tolerated. Said sampling frequency, like others present in the system, shall be therefore considered as an example only.

The outgoing numeric signal (1.9) from sampler (1.7) is then frequency corrected through the four-correlator frequency recovery circuit (Automatic Frequency Control, AFC) (1.10) (Subsystem A1).

Signal (1.12) at the output of the subsystem A1 is filtered by anti-aliasing filter (1.11), is decimated at frequency 2/T in block (1.13) and then is further corrected by digital mixer (1.20) to provide signal (1.19). Mixer (1.20) is part of subsystem A2 and is driven by the joint frequency and phase locked loop (1.14) labelled JFPLL in the figure, which uses the signal (1.17) at the input of the decision element (1.16) and the decided data (1.18) made available at its output. Signal (1.19) is processed by subsystem C) (1.15), labelled SHAPING AND EQUALIZATION in the figure, to output signal (1.17).

The following is a more detailed description of the automatic frequency control block (the heart of subsystem A1) labelled AFC in the figure, the clock recovery loop block (included in subsystem B) labelled CRL in the figure, the shaping and equalization subsystem C) and the joint frequency and phase locked loop block labelled JFPLL in the figure.

* Description of AFC block

AFC indicates the four-correlator circuit for recovering the frequency error whose block diagram is illustrated in fig. 2.

According to one aspect of the invention the system is realized through the use of a feedback loop that, from the processing of samples of the complex signal (2.1) (coinciding with signal 1.12 of fig. 1) at the input of the anti-aliasing filter (2.2) (coinciding with block 1.11 in fig. 1) estimates and corrects the residual frequency error of the baseband conversion operation.

In order to obtain such result the following operations on the signal are necessary:

- the samples of the complex signal (2.1) are processed at frequency 4/T by the frequency error detector (2.3) realized with a balanced four-correlator which outputs a real signal (2.4) Proportional to the estimated frequency error;
- the samples of the error signal (2.4) from the frequency error detector are averaged in block (2.5) and presented at frequency 1/T to the loop filter (2.6) where they are filtered;
- the samples (2.7) from the loop filter (2.6) are read at frequency 4/T by block (2.8) and then integrated (2.9);
- the integrator output (2.10) is used for addressing a table (2.11) that provides the correction complex signal (2.12) to digital mixer (2.13) which processes signal (2.14) (coin-

ciding with signal 1.9 in fig. 1).

*** Description of CRL block**

Reference CRL (Clock Recovery Loop) indicates the circuit for recovering the synchronism of symbol whose block diagram is shown in fig. 3.

According to one aspect of the invention, the system is realized through a feedback loop. The samples of the complex signals (3.1) at frequency 2/T (coinciding with signal 1.19 of fig. 1) are processed to provide the signal (3.7) that drives the sampling circuit (3.8) (coinciding with block 1.7 in fig. 1) at frequency 4/T.

In order to obtain such a result the following operations on the signal are necessary:

- the complex signal (3.1) is processed by clock error detector (3.2) according to a maximum power algorithm, that provides the real signal (3.3) proportional to the time reference error;
- in an embodiment, the signal (3.3) is then filtered by the digital loop filter (3.4) whose output (3.5) is used for driving a numerically controlled oscillator (3.6) that outputs the square wave with a frequency of 4/T (3.7) that is applied to sampler (3.8).

*** Description of the SHAPING AND EQUALIZATION block**

The block labelled SHAPING AND EQUALIZATION performs the shaping of the signal and the adaptive equalization; according to another aspect of the invention, the block diagram relative to this subsystem C) is represented in fig. 4.

In such block the complex signal (4.1), coinciding with signal (1.19) in fig. 1, is at first filtered by the matched filter (4.2) realized through a finite impulse response (FIR) filter. Signal (4.3) is then decimated at frequency 1/T in block (4.4) and hence equalized in block (4.5). The equalizer outputs signal (4.6) coinciding with signal (1.17) in fig. 1. Inserted in the equalization block (4.5) is also the coefficient updating device that operates in accordance with an algorithm insensitive to phase and frequency of the incoming signal.

*** Description of JFPLL block**

Reference JFPLL (Joint Frequency and Phase Locked Loop) indicates the circuit for recovering both frequency and phase error whose block diagram is illustrated in fig. 5.

Still according to one aspect of the invention, the system is realized by a feedback loop which, by suitably processing the samples 5.1 (coinciding with signal 1.18 in fig. 1), estimates and corrects the residual phase and frequency error of the recovery operation performed by AFC.

In order to obtain such result the following operations on signals are necessary:

- the samples of the complex signal (5.1) and the estimates of the complex symbols (5.3) are processed at frequency 1/T by the frequency phase error detector (5.4) that outputs two real signals (5.5) and (5.6) respectively proportional to frequency error and phase error;
- the samples of signals (5.5) and (5.6) are then filtered respectively by the frequency recovery (FR) filter (5.7) and by the phase recovery (PR) filter (5.8); the outputs (5.9) and (5.10) of such filters are then suitably added in the adder (5.11);
- the outgoing samples (5.12) from adder (5.11) are read at frequency 2/T by block (5.13) and then integrated (5.14);
- the output (5.15) of the integrator is used for addressing a table (5.16) that provides the correction complex signal (5.17) to digital mixer (5.18), coinciding with mixer (1.20) of fig. 1.

Even if the invention has been described with reference to the embodiments represented in the drawings for simplicity and clearness' sake, it is susceptible to those variations and replacements which, being within the reach of those skilled in the art, are to be considered as naturally falling within the scope and in the spirit of the present invention.

Claims

1. System for demodulating numeric signals with QAM modulation, including:
   A) a subsystem for recovering the frequency and the phase of the carrier,
   B) a subsystem for the reconstruction of the synchronism of the symbol capable of driving the signal sampling circuit, and
   C) a subsystem constituted by filters,
   characterized in that
   a) subsystem A) in turn includes a four-correlator carrier frequency recovery subsystem A1, and a subsystem A2 for the joint recovery of phase and frequency of the carrier which uses the estimated data;
   b) subsystem B) uses the signal at the input of subsystem C) and comprises the circuit (placed upstream of subsystem A1) used for sampling the signal entering the system and converting it into a numeric one;
   c) subsystem C) comprises a fixed digital filter which completes the shaping of the transmitted pulse and an adaptive digital equalizer.

2. System according to claim 1, characterized in that placed at its input is a free oscillator for the baseband conversion.

3. System according to claim 1, characterized in that subsystem A) for the carrier recovery and the baseband conversion,
comprises:
a1) a four-correlator loop for the carrier frequency recovery and
a2) a joint phase and frequency recovery loop that uses the decided data.

4. System according to claim 1, characterized in that subsystem B) operates the reconstruction of the synchronism of symbol with a maximum power criterion applied to the signal at the input of subsystem C).

5. System according to claim 1, characterized in that the shaping and equalization circuit C) comprises a shaping FIR filter and an equalization adaptive FRI filter whose coefficients are updated through a criterion insensitive to the input signal phase.

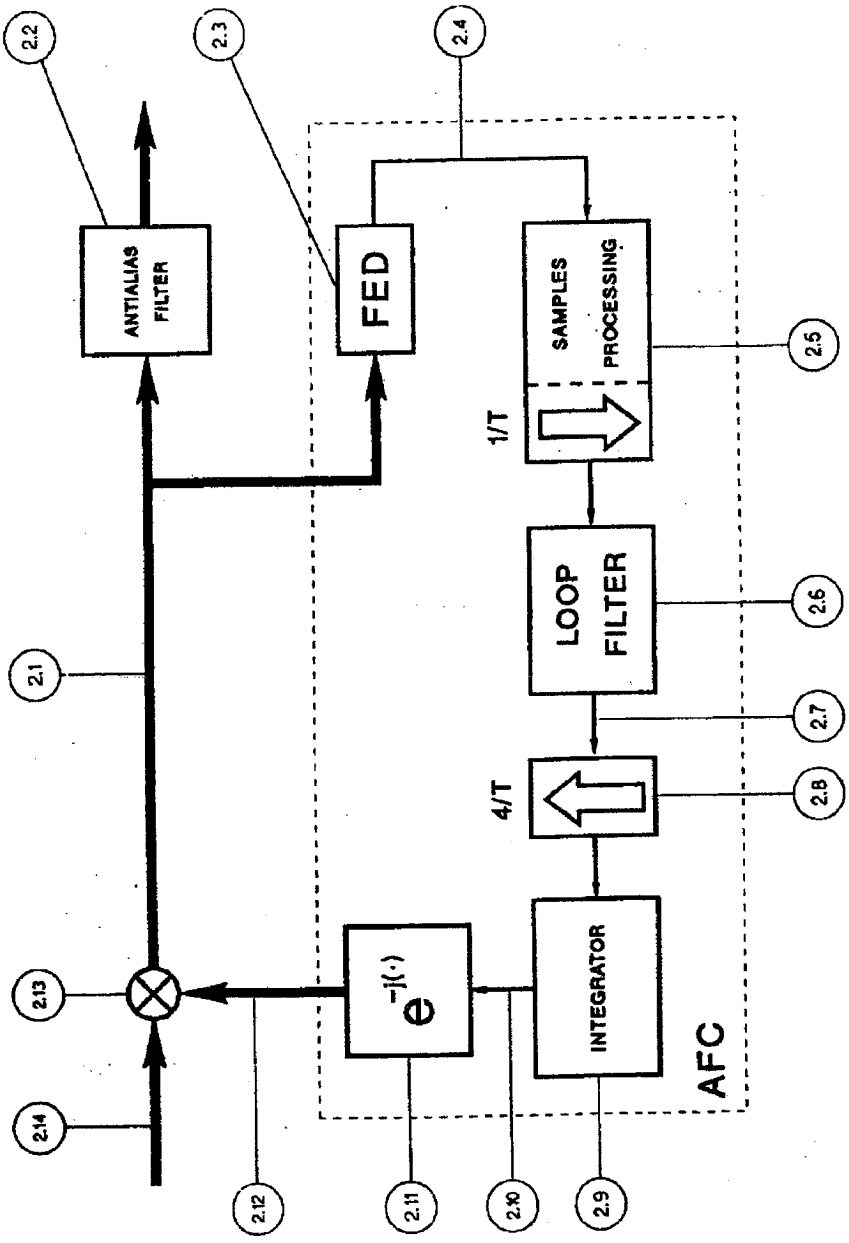
2.2
2.3
2.4
ANTIALIAS FILTER
FED
SAMPLES PROCESSING
2.5
1/T
LOOP FILTER
2.6
2.1
2.7
4/T
2.8
2.13
$e^{-j(\cdot)}$
INTEGRATOR
AFC
2.14
2.12
2.11
2.10
2.9

Fig. 2